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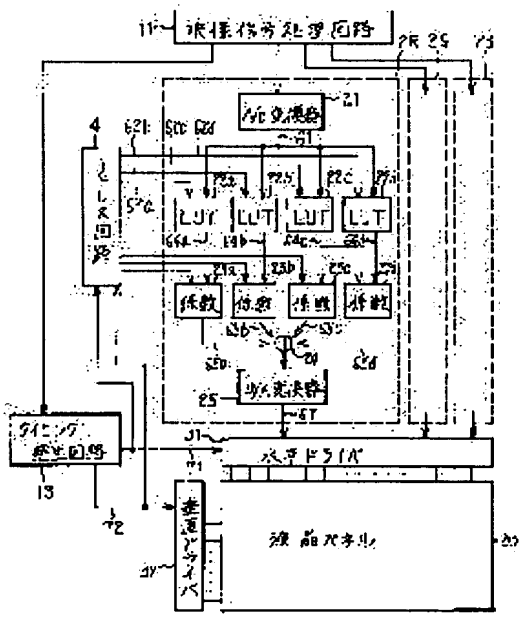
(54) VIDEO SIGNAL CORRECTION DEVICE AND DISPLAY DEVICE USING THE SAME

(57)Abstract:
PURPOSE: To reduce the memory capacity of an LUT used for the video signal correction device implementing gamma correction and to reduce uneven brightness caused in the liquid crystal display device.
CONSTITUTION: A display pattern is divided into blocks and gamma correction data for each of some blocks are stored in LUT22a,22b,22c,22d A video signal 61d converted into a digital signal by an A/D converter 21 is inputted to the four LUTs and the result is given to an interpolation circuit comprising coefficient provision circuits 23a,23b, 23c,23d and an adder circuit 24, in which a video signal of a block having no gamma correction data is generated.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The A/D converter which outputs the video-signal data which carried out digital conversion of the video signal, The address circuit which outputs the level pixel location data in which the block location which inputted the horizonatl driving pulse and vertical driving pulse which are formed of a timing generating circuit from a synchronizing signal, and carried out screen separation on the display screen is shown, and perpendicular pixel location data, On an upper address line, said level block location data and said perpendicular block location data, Two or more look-up tables which consider the video signal of said A/D-converter output as an input, and store display unevenness amendment data in a lower address line for two or more blocks of every, The video-signal compensator characterized by having the interpolation processing circuit which consists of a multiplier addition circuit which considers as an input two or more amendment video-signal data outputted from said two or more look-up tables, and an adder.
[Claim 2] The display using said video-signal compensator according to claim 1.
[Claim 3] The video-signal compensator by which two or more look-up tables of said video-signal compensator according to claim 1 are constituted from RAM, and said RAM is connected with external storage, such as ROM, and a floppy disk, a hard disk, with the data bus.
[Claim 4] The data bus of a video-signal compensator according to claim 3 is a microcomputer and a connectable video-signal compensator.
[Claim 5] The A/D converter which outputs the video-signal data which carried out digital conversion of the video signal, The first look-up table which carries out visibility amendment of the output digital video signal of said A/D converter, The address circuit which outputs the level pixel location data in which the block location which inputted the horizonatl driving pulse and vertical driving pulse which are formed of a timing generating circuit from a synchronizing signal, and carried out screen separation on the display screen is shown, and perpendicular pixel location data, On an upper address line, said level block location data and said perpendicular block location data, Two or more second look-up tables which consider the video signal of said first look-up table output as an input at a lower address line, and store display unevenness amendment data for two or more blocks of every, The interpolation processing circuit which consists of a multiplier addition circuit which considers as an input two or more amendment video-signal data outputted from said two or more second look-up tables, and an adder, The video-signal compensator characterized by having the third look-up table which considers the output of said interpolation processing circuit as an input, and carries out a gamma correction.
[Claim 6] The video-signal compensator which changes the data of said third look-up table of said video-signal compensator according to claim 5 according to the contents of a display.
[Claim 7] The display using said video-signal compensator according to claim 6.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the video-signal compensator which amends electrically the brightness unevenness generated on dot-matrix form displays, such as a liquid crystal display, and the display using it.
[0002]
[Description of the Prior Art] After changing the inputted analog picture signal into a digital signal in the liquid crystal display using a active matrix, For example, the look-up table (it omits Following LUT) which consists of memory is used. Change an input video signal into the liquid crystal applied-voltage signal doubled with the liquid crystal display property. The gamma correction data in the LUT are switched according to an image display location, and realizing a liquid crystal display with little brightness unevenness is shown in JP,3-18822,A at the same time it performs the so-called gamma correction.
[0003]
[Problem(s) to be Solved by the Invention] The above-mentioned conventional technique divided the display screen on a liquid crystal panel into the suitable block, and has switched gamma correction data per block. At this time, for example, a digital image signal, it consists of 8 bits per pixel (zero to 255 gradation), and when it assumes that there was about 75% of brightness of a periphery to the center section of the screen further, the amendment for brightness difference 25% (64 gradation) of a center section and a periphery is needed. In order to prevent the problem that the brightness difference of the joint (border area) of a block arises and is conspicuous with the difference of the gamma correction curve during a block, 64 blocks is divided from a center section to a periphery, and, as for the amendment during a block, it is desirable that it is ground-floor tone extent. that is, the horizontal and the perpendicular divided the whole display screen into 128 -- 128x 128= 16,384 blocks are needed. It is LUT if the 8-bit gamma correction data for 256 gradation need by three primary colors for every block. Thing mass data were needed by 16,384x256x8x3=96Mbit, and there was a problem that a price was high (the unit of 1024 bit=1Kbit and 1024Kbit=1Mbit shows memory space according to the practice).
[0004] Then, this invention is to offer the video-signal compensator of a low price and the dot-matrix form display using it which interpolated brightness unevenness amendment combination gamma correction data, in order to realize brightness unevenness reduction and a gamma correction by small memory space.
[0005]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention stores gamma correction data for some of every blocks, and the interpolation data obtained from the data of the block with nearby gamma correction data by carrying out data processing are used for the data of the block without gamma correction data.
[0006] furthermore, each brightness unevenness amendment data -- the difference from the main gamma correction data -- by storing as information, when compressing the brightness unevenness amendment data per block and using it as gamma correction data, much more memory space reduction is aimed at by carrying out data processing and reproducing the original data.
[0007]
[Function] For example, gamma correction data are stored every 4x4 blocks, and brightness unevenness amendment can be realized by 1/16 of conventional memory space from substituting interpolation data for the gamma correction data of other blocks. Since it is thought from the first that the brightness difference of the gamma correction data of a contiguity block is ground-floor tone extent, and there is no big change of gamma correction data in about 16 blocks in order not to highlight the boundary during each block, it is

thought that it is rare for the brightness unevenness amendment effectiveness by the above-mentioned interpolation data use to decrease.
[0008] furthermore, the difference to the gamma correction data of a large block of gamma correction data when there is no big difference in the gamma correction data during a block in every 16x16 block (it is hereafter called a large block) -- information is stored in every 4x4 block (it is hereafter called an inside block). case 8 bits is required as gamma correction data -- difference -- since it can express by about 4 bits as information, compared with the case where gamma correction data are stored in all inside blocks, there is effectiveness which can reduce memory space by half mostly further.
[0009]
[Example] Hereafter, as an example of a dot-matrix form display, a liquid crystal display is taken up, and the video-signal compensator of one example of this invention and the display using it are explained, referring to a drawing.
[0010] Drawing 1 shows the block diagram of the video-signal compensator in the first example of this invention, and the liquid crystal display using it. For an A/D converter, 22a, and 22b, 22c, and 22d, in drawing 1 , LUT, 23a, and 23b, 23c, and 23d of a multiplier addition circuit and 24 are [2R, 2G, the video-signal compensator corresponding to / for example / the three-primary-colors video signal of R (red) G (green), and B (blue) in respectively 2B, and 21 / an adder and 25] D/A converters.
[0011] It is outputted from the video-signal processing circuit 11 which creates an analog three-primary-colors video signal, a horizontal, and a Vertical Synchronizing signal from a video signal, and the video signal 61 by which digital conversion was carried out is inputted into juxtaposition with A/D converter 21 in an LUTs [22a, 22b, 22c, and 22d] lower address at 8 bits. On the other hand, a horizontal and a Vertical Synchronizing signal create a horizonatl driving pulse 71 and a vertical driving pulse 72 in the timing generating circuit 13. A liquid crystal panel 33 is driven by the level driver 31 controlled by the horizonatl driving pulse 71, and the perpendicular driver 32 controlled by the vertical driving pulse 72.
[0012] At this time, the address circuit 4 creates the level block location data and perpendicular block location data in which the block location which carried out screen separation is shown from a horizonatl driving pulse 71 and a vertical driving pulse 72, and the LUT control signals 62a, 62b, 62c, and 62d based on that block location data are inputted into it by the LUTs [22a, 22b, 22c, and 22d] upper address. Consequently, when LUTs 22a, 22b, 22c, and 22d refer to a table, the video signals 64a, 64b, 64c, and 64d for 4 blocks by which the gamma correction was carried out to the digital video signal 61 given to the lower address are acquired. To coincidence, based on block location data, the address circuit 4 gives the multiplier selection signals 63a, 63b, 63c, and 63d to the multiplier addition circuits 23a, 23b, 23c, and 23d, and acquires the signals 65a, 65b, 65c, and 65d which multiplied the predetermined multiplier to a multiplier selection signal by the video signals 64a, 64b, 64c, and 64d for 4 blocks. The display image by which the digital video signal 66 by which the gamma correction was carried out with interpolation by adding these signals to an adder 25 and adding corresponding to the block location was acquired, and this was changed by the analog signal with D/A converter 25, was inputted into the level driver 31, and brightness unevenness amendment was carried out for every block on the liquid crystal panel at a gamma correction and coincidence is obtained.
[0013] About the video-signal compensator constituted as mentioned above, the actuation is explained below.
[0014] Drawing 2 is drawing explaining the principle of operation which acquires the digital video signal to which the gamma correction of the predetermined block was carried out by interpolation from 4 blocks with gamma correction data which approached in an example. i and j show perpendicularity and a level block location, respectively, and show the location for a block with the coordinate of (i, j) hereafter. O mark is entered in level and the block for 4 blocks of every perpendiculars with gamma correction data. namely, 4x -- the memory space which stores gamma correction data in all blocks by having gamma correction data every 4= 16 blocks compared with the conventional method of giving gamma correction data -- about -- it can decrease to 1/16. That is, since it ends with 32x32=1,024, the block which has gamma correction data when it has the block of 128x128=16,384 explained in the conventional example is the sum total memory space of four LUTs 22a, 22b, 22c, and 22d. It doubles by 1,024x256x8=2Mbit (per each LUT, 0.5Mbit), and three primary colors. 2Mbitx3=6Mbit It can decrease.
[0015] Next, how to search for the digital video signal eij with which the gamma correction of the block without gamma correction data (i, j) was carried out with interpolation is explained.
[0016] LUTs 22a, 22b, 22c, and 22d presuppose that the gamma correction data of a block of (8m+4, 8n), (8m, 8n+4), and (8m+4, 8n+4) are stored, respectively (8m, 8n) (however, m and n zero or more integers).

At this time, it is 0<=i and j<=4. In the range, the gamma correction data of four blocks (0 0) close to a block (i, j), (0, 4), (4, 0), and (4, 4) are used. (i, j) Digital video signals a00, b04, c40, and d44 over the input video signal of a block by which the gamma correction was carried out It obtains from LUTs 22a, 22b, 22c, and 22d. At this time, the digital video signal eij by which the gamma correction was carried out is searched for from a formula (1) by 2-dimensional linear interpolation.

[0017]

[Equation 1]

[数1]

$$e_{ij} = \frac{1}{16}\{(4-i)(4-j)a_{00} + (4-i)j\,b_{04} + i(4-j)c_{40} + ij\,d_{44}\}$$

(但し. $0 \leq i, j \leq 4$)

---- (1)

[0018] Namely, digital video signals a00, b04, c40, and d44 After multiplying a predetermined multiplier, respectively, by adding shows that the digital video signal eij by which the gamma correction was carried out is acquired. The circuits which perform this data processing were the multiplier addition circuits 23a, 23b, 23c, and 23d and an adder 24. Next, actuation of a multiplier addition circuit is taken up for an example, and multiplier addition circuit 23a is explained.

[0019] As shown in drawing 1 , it is the circuit which obtains the output data which output video-signal 64of LUT22a a (equivalent to a video signal a00 and a08 in drawing 2) and multiplier selection-signal 63a of an address circuit are inputted into multiplier addition circuit 23a, and are equivalent to the first term in a formula (1). Drawing 3 is drawing in which summarizing these relation and showing the output data of multiplier addition circuit 23a in the first example. What is necessary is to be able to realize a multiplier addition circuit by memory etc. like LUT, and just to give every 3 bits [of low order of the addresses i and j which show a block location to a lower address for 8 bit video-signal 64a which changes to video signals a00, a08, and a80 etc. according to a block location] a total of 6 bits to an upper address. Memory space which constitutes multiplier addition circuit 22a in the configuration of this 14-bit address and 8-bit data It is [16Kbitx8=128Kbit] necessary. this time -- the memory space of LUT -- doubling -- 2Mbit+128Kbitx4=2.5Mbit and three-primary-colors part 2.5 in all Mbitx3=7.5Mbit it is -- even if it thinks by the whole system -- 96Mbit of the conventional example Sharp reduction can be compared and carried out.

[0020] Now, when drawing 3 is seen, the multiplier required of a multiplier addition circuit is 0, 1/1 / 3 / 1 / 3 / 1 / 9 / 3 / 1. It turns out that there are only ten kinds. [16 and 1] [8 and 3] [16 and 1] [4 and 3] [8 and 1] [2 and 9] [16 and 3] [4 and 1] Therefore, since it ends with a total of 64 kinds of every 3 bits [of low order of the addresses i and j which show the block location at the time of constituting a multiplier addition circuit from memory by devising a multiplier selection signal] multiplier selection signals [6-bit], and ten kinds, it is the memory space of a multiplier addition circuit. It can decrease to one sixth so much to 256x10x8=20Kbit and above-mentioned 128Kbit. Hereafter, based on this memory space reduction technique, the concrete circuitry and actuation of the address circuit 4 in the example of drawing 1 , and actuation of the multiplier addition circuits 23a, 23b, 23c, and 23d are explained.

[0021] Drawing 4 is the block diagram showing the example of a configuration of the address circuit in the first example. The horizonatl driving pulse 71 and vertical driving pulse 72 which are the output signal of the timing generating circuit of drawing 1 , respectively are given to input terminals 49h and 49v, and level block pulse 73h and perpendicular block pulse 73v are obtained with counting-down circuits 41h and 41v to them. By carrying out dividing of the level block pulse 73h by 42h of four counting-down circuits, and 43h of two counting-down circuits, 74h of 3 bit signals of low order of the level block location j is acquired, and a Decoders [46a, 46b, 46c, and 46d] lower address is given. Similarly, by carrying out dividing of the perpendicular block pulse 73v by 4 counting-down-circuit 42v and 2 counting-down-circuit 43v, 3 bit signal 74of low order v of the perpendicular block location i is obtained, and a Decoders [46a 46b, 46c, and 46d] upper address is given. Decoders 46a, 46b, 46c, and 46d acquire the multiplier selection signals 63a, 63b, 63c, and 63d of 4 bits of each which is given to the multiplier addition circuits 23a, 23b, 23c, and 23d from the 3 bit signals 74h and 74v of low order of a horizontal and the perpendicular block locations i and j.

[0022] The output signal of 43h of two counting-down circuits is carried out 16 dividing by 44h of further 16 counting-down circuits, and uses 75h of 4 bit signals of high orders of the level block location j as a low

order control signal of the LUT control signals 62a and 62c of LUTs 22a and 22c. 76h of signals which delayed 75h of 4 bit signals of high orders of the level block location j at 45h of delay circuits is used as a low order control signal with an LUT control signals [62b and 62d] of LUTs [22b and 22d]. the block with which the gamma correction data which, as for using a delay circuit, each LUT has gamma correction data for every 8 level block, and LUTs 22b and 22c store to LUTs 22a and 22c correspond -- 4 level block gap ****** -- things are supported. Similarly, the output signal of 2 counting-down-circuit 43v is carried out 16 dividing of further 16 counting-down circuits by 44v, and uses 4 bit signal 75of high orders v of the perpendicular block location i as a high order control signal of the LUT control signals 62a and 62b of LUTs 22a and 22b. Signal 76v which delayed 4 bit signal 75of high orders v of the level block location i by delay circuit 45v is used as a low order control signal with an LUT control signals [62c and 62d] of LUTs [22c and 22d].

[0023] Table 1 is drawing showing the multiplier selection-signal input of a multiplier addition circuit, and correspondence of the ten above-mentioned kinds of multipliers.

[0024]

[Table 1]

[表1] 係数付加回路の係数選択信号と係数の対応を示す表

係数選択信号	0	1	2	3	4	5	6	7	8	9	10～15
係数	0	1/16	1/8	3/16	1/4	3/8	1/2	9/16	3/4	1	—

[0025] In order to choose ten kinds of multipliers, the 4-bit multiplier selection signal is used, and this is equivalent to the multiplier selection signals 63a, 63b, 63c, and 63d of drawing 4 . Thus, by setting, the circuit scale of a multiplier addition circuit can be set to 20Kbit as above-mentioned. Based on the output data of multiplier addition circuit 23a of drawing 3 , the multiplier selection signal of Table 1 is used, it is Table 2 which showed a perpendicular and the level block locations i and j, and the relation of a multiplier selection signal, and this serves as an I/O table of decoder 46a. Similarly, a Decoders [46b 46c, and 46d] I/O table is called for as shown in Table 3, Table 4, and Table 5.

[0026]

[Table 2]

[表2] デコーダ46aの出力を示す表

I \ J	0	1	2	3	4	5	6	7
0	9	8	6	4	0	4	6	8
1	8	7	5	3	0	3	5	7
2	6	5	4	2	0	2	4	5
3	4	3	2	1	0	1	2	3
4	0	0	0	0	0	0	0	0
5	4	3	2	1	0	1	2	3
6	6	5	4	2	0	2	4	5
7	8	7	5	3	0	3	5	7

[0027]

[Table 3]

[表3] デコーダ46bの出力を示す表

I \ J	0	1	2	3	4	5	6	7
0	0	4	6	8	9	8	6	4
1	0	3	5	7	8	7	5	3
2	0	2	4	5	6	5	4	2
3	0	1	2	3	4	3	2	1
4	0	0	0	0	0	0	0	0
5	0	1	2	3	4	3	2	1
6	0	2	4	5	6	5	4	2
7	0	3	5	7	8	7	5	3

[0028]
[Table 4]
[表4] デコーダ46cの出力を示す表

I \ J	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	4	3	2	1	0	1	2	3
2	6	5	4	2	0	2	4	5
3	8	7	5	3	0	3	5	7
4	9	8	6	4	0	4	6	8
5	8	7	5	3	0	3	5	7
6	6	5	4	2	0	2	4	5
7	4	3	2	1	0	1	2	3

[0029]
[Table 5]
[表5] デコーダ46dの出力を示す表

I \ J	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	0	1	2	3	4	3	2	1
2	0	2	4	5	6	5	4	2
3	0	3	5	7	8	7	5	3
4	0	4	6	8	9	8	6	4
5	0	3	5	7	8	7	5	3
6	0	2	4	5	6	5	4	2
7	0	1	2	3	4	3	2	1

[0030] Since these decoders can be realized also as an LUT which used memory and the address is [a total of 6 bits and the output data of 3 bits of low order of a perpendicular and the level block locations i and j of the memory space at this time] 4 bits, it is 64x4=256bit. It becomes.
[0031] the case where the block of 128x128 is used when the above result was summarized -- the first example -- setting -- memory space required for per Isshiki -- LUT 0.5Mbitx3=2Mbit and multiplier addition circuit 20Kbitx4=80Kbit and address addition circuit 256x4=1Kbit A total of 2.1 Mbit it is -- even if it takes into consideration a part for three primary colors 2.1Mbitx3=6.3Mbit It can constitute. Thus, about 1/of memory reduction of 16 can be aimed at to 96Mbit of the conventional example.
[0032] The block diagram of the video-signal compensator of the second example of this invention and the indicating equipment using it is shown in drawing 5 , and it explains hereafter, referring to a drawing.
[0033] In the first example, each LUT had 8-bit output data. However, as mentioned above, the gradation change during a contiguity block is 0 - 1 gradation extent, even when it has gamma correction data every 16 blocks for level and 4 blocks of every perpendiculars, is carried out to the gradation change in every 16

blocks, and is considered to be 0 - 4 gradation extent. Therefore, if the whole of each LUT does not need to have 8 bits (256 gradation) output data and it has gamma correction data of difference, memory space can be reduced further. the second example -- difference -- memory space by the activity of data is planned.
[0034] That the block diagram of drawing 5 differs from the block diagram of drawing 1 greatly are the point that LUT26 inputted into an adder 24 without passing along a multiplier addition circuit is added, and a point with less LUTs [22a, 22b, 22c, and 22d] output-data width of face than 8 bits which consists of 4 bits, for example.
[0035] LUT26 shall consider 6 bits of high orders of the digital video signal 61 as an input by making into a unit the large block which consists of 13 blocks of horizontal 13x perpendiculars, and shall have rough gamma correction data with an output-data width of face of 6 bits. the inside of a large block -- setting -- every four difference [a total of 16] per level and 4 blocks of perpendiculars -- gamma correction data -- LUTs 22a, 22b, 22c, and 22d -- having -- the difference of each block with the same interpolation as the first example -- a gamma correction signal is acquired. difference -- a gamma correction signal is between contiguity blocks, and since it is considered that there is little gradation change, it is good by output width of face of about 4 bits as mentioned above. the signal which made the output of LUT26 6 bits of high orders, and set 2 bits of low order to 0 with the adder 24 -- the above-mentioned difference -- the digital video signal by which added the gamma correction signal and the gamma correction was carried out for every block is acquired. Supposing the display screen is divided into the block of 128x128, when a horizontal and a perpendicular repeat this actuation about a total of every 100 ten-piece blocks [large], the digital video signal by which the gamma correction was carried out about the whole block will be acquired in the large block which consists of 13x13 blocks.
[0036] Next, the memory space in the example of drawing 5 is calculated. Since the input video signal of LUT26 is output-data width of face of 6 bits in 6 bits in a large block 64x6=384bit It is memory space. Since large block Nakamizu common and the perpendicular which an input video signal is 4 bits in output-data width of face in 8 bits, and consists of 13x13 blocks are every 4 blocks and it is necessary to prepare it 4= 16 kinds of level 4x perpendiculars, LUTs 22a, 22b, 22c, and 22d are 256x4x16=16Kbit. It becomes memory space. Since there are 100 large blocks in the whole display screen, it is only LUT relation. (384 bit+16Kbit) It is set to x100=1.64Mbit. Since the data width of face treating a multiplier addition circuit is the one half of the first example, 40Kbit and an address circuit are almost equal to the first example, and it is 1Kbit. At the whole, memory space can be further reduced compared with 5.1Mbit and the first example by 1.7Mbit and three classification by color per Isshiki.
[0037] The block diagram of the video-signal compensator of the third example of this invention and the indicating equipment using it is shown in drawing 6 , and it explains hereafter, referring to a drawing.
[0038] In the first example, in order to perform brightness unevenness amendment to a gamma correction and coincidence, the block with gamma correction data had data in the form containing all of both of brightness unevenness amendments and gamma corrections. then -- the third example -- a brightness unevenness amendment function and a gamma correction function -- dissociating -- brightness unevenness amendment data -- difference -- memory space reduction is aimed at by considering as data.
[0039] Usually, the output signal of the video-signal processing circuit 11 is a thing corresponding to the display property of the Braun tube (CRT), and it is the signal with which the so-called reverse gamma correction was applied in many cases so that the image seen through the Braun tube may look natural. The video-signal electrical-potential-difference differences sensed that this signal by which the reverse gamma correction was carried out differs from the visibility property, was seen with the naked eye, and brightness changed differ a black display and near a white display. Therefore, in order to realize brightness unevenness amendment by small memory space, it sees with the naked eye, amendment which becomes equal in a black display, a white display, and a halftone display about the video-signal electrical-potential-difference difference sensed that brightness changed is applied beforehand, and the method of performing brightness unevenness amendment is best. Then, what is necessary is to perform the gamma correction doubled with the display property of a display device, and just to drive a display device.
[0040] That the block diagram of drawing 6 differs from the block diagram of drawing 1 greatly are the point that LUT27 was inserted in the output of A/D converter 21, the point that the output 68 of LUT27 was applied also to the adder 24, and the point that LUT28 was further inserted in the output of an adder 24.
[0041] LUT27 forms the daisy ITARU video signal 68 which is 8 bits, and is inputted into LUTs 22a, 22b, 22c, and 22d with brightness unevenness amendment data so that the gradation difference and digital video-signal difference which look at and sense the digital image output signal of A/D converter 21 with the digital video signal by which visibility amendment was carried out, i.e., a naked eye, may be proportional mostly.

since the digital video signal 68 by which visibility amendment was carried out is added to the adder 25 -- as brightness unevenness amendment data -- difference -- information is sufficient, for example, if it is going to amend 25% of brightness difference by the center section and the periphery, it will end by about 6 bits as data width of face. About formation actuation of the brightness unevenness amendment data by which each block was interpolated, it is the same as that of the first example, and detailed explanation is omitted.

[0042] From an adder 25, the digital video signal 66 by which brightness unevenness amendment was carried out with visibility amendment is outputted, and it is given to LUT28. LUT28 is the video signal by which the gamma correction was carried out to brightness unevenness amendment by performing the gamma correction in consideration of the display property of the liquid crystal panel used as a display device, and driving D/A converter 25, and drives a liquid crystal panel through a level driver, and good image display is obtained.

[0043] Next, the memory space in the example of drawing 6 at the time of dividing a screen into the block of the level 128x perpendicular 128 is calculated. Since the input video signal of LUT27 and LUT28 is output-data width of face of 8 bits in 8 bits, respectively 256x8=2Kbit It is memory space. Since an input video signal is 6 bits in output-data width of face in 8 bits, and level and a perpendicular are every 4 blocks and it is necessary to prepare it 32= 1,024 kinds of level 32x perpendiculars, LUTs 22a, 22b, 22c, and 22d are 256x6x1,024=1.5Mbit. It becomes memory space. Since the data width of face treating a multiplier addition circuit is 6/8 of the first example, 60Kbit and an address circuit are almost equal to the first example, and it is 1Kbit. Therefore, at the whole, memory space can be further reduced compared with 4.8Mbit, the first, or the second example by 1.6Mbit and three classification by color per Isshiki.

[0044] Furthermore, in the third example, some data of LUT28 are prepared, for example, there is effectiveness which can perform easily changing a gradation display property according to a movie and the contents of a display, such as news.

[0045] Moreover, although the digital video signal 68 by which visibility amendment was carried out using LUT27, i.e., a daisy ITARU video signal with which the gradation difference seen and sensed with the naked eye is proportional to a digital video-signal difference mostly, was formed in the third example, LUT27 can also be excluded by performing this processing in analog in a video-signal processing circuit. Since it sees with the naked eye and the gradation difference and video-signal difference to sense are proportional mostly at this time, the dynamic range of an A/D converter can be used most effectively. In addition, it is in ** that the display property of a display device can omit LUT28 when almost equal to visibility. The block diagram of the indicating equipment of the fourth example of this invention is shown in drawing 7 , and it explains hereafter, referring to a drawing.

[0046] It is related with the amendment data storage approach from the first described so far to LUT of the indicating equipment using the third example. Generally these LUTs can be realized comparatively easily by constituting from ROMs, such as EPROM and EEROM. However, the high-speed access time ROM of 60 - 30nS extent required for the digital video signal which synchronized with the 15-30MHz clock, for example is not easy to receive. Then, the data stored in 81 constituted from a low speed EPROM by LUT, using RAM, such as a comparatively high-speed static RAM, are used as the system transmitted to RAM 82 and 83 at the power up of a display etc. It has the data bus 85 to which RAM 82 and 83 and EPROM81 as an LUT are connected for this data transfer. In case display properties, such as brightness unevenness of a display and gradation display nature, are adjusted to this data bus, when connection of a microcomputer 86 is enabled as an adjustment fixture, it is convenient for it. Furthermore, it connects with a luminance meter 87, TV camera 88, etc., and a microcomputer has the advantage which can attain automation of display property adjustment. Furthermore, a comparatively mass thing is obtained by the low price, and a low speed EPROM also has the advantage which can choose a gradation display property by preparing two or more gamma correction data, and transmitting the optimal gamma correction data to RAM as an LUT from a cheap thing, to a display screen. Moreover, although explained having stored gamma correction data in ROM81, even if it is not ROM, it is in ** that bulk memories, such as a floppy disk and a hard disk, can be substituted.

[0047] As mentioned above, as a dot-matrix form display, although the liquid crystal display was mentioned and explained to the example and was come to it, even if it uses for other EL (electroluminescence), PDP (plasma display), VDP (fluorescent indicator tube), etc., there is same effectiveness.

[0048]

[Effect of the Invention] While reducing brightness unevenness by comparatively small memory space according to this invention, the video-signal compensator which can form the video signal by which the gamma correction was carried out is realizable. Furthermore, there is little brightness unevenness, a

gradation display property is good, and since the gradation display property of having been suitable for the contents of a display image can be chosen, a display with a feeling of high definition is realizable according to the display using the video-signal compensator of this invention.

[Translation done.]

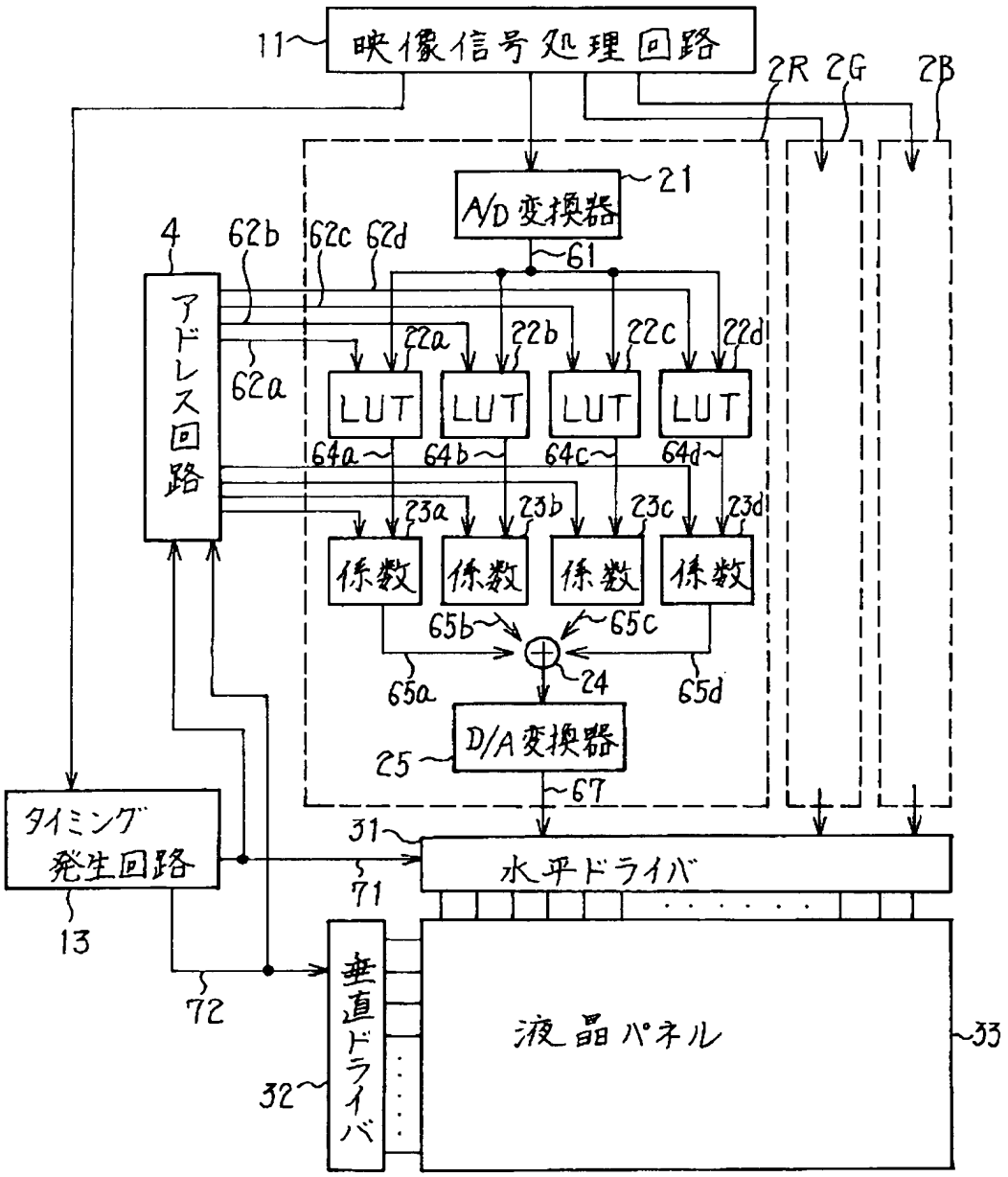
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

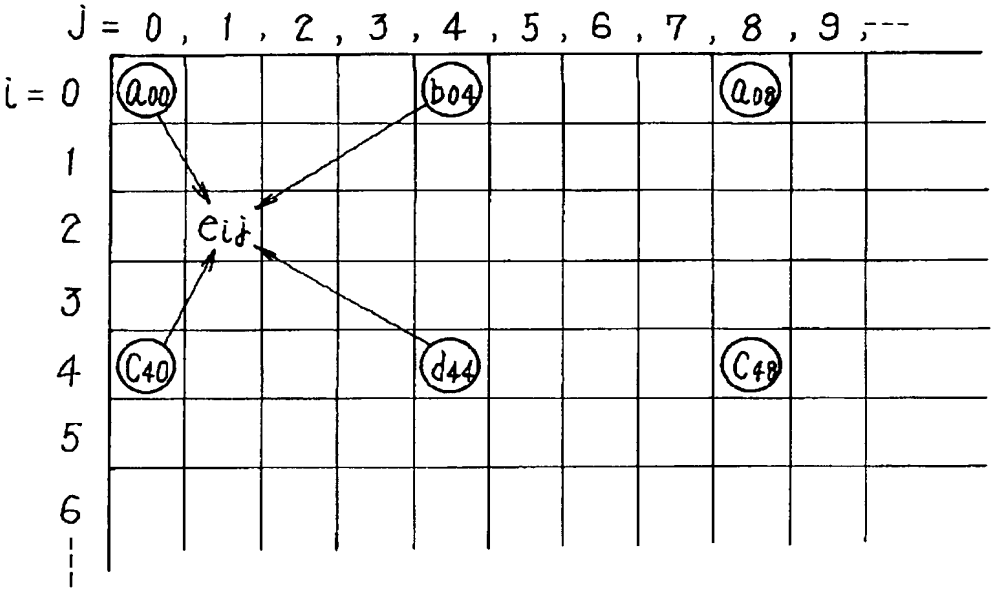
[Drawing 1]

図 1



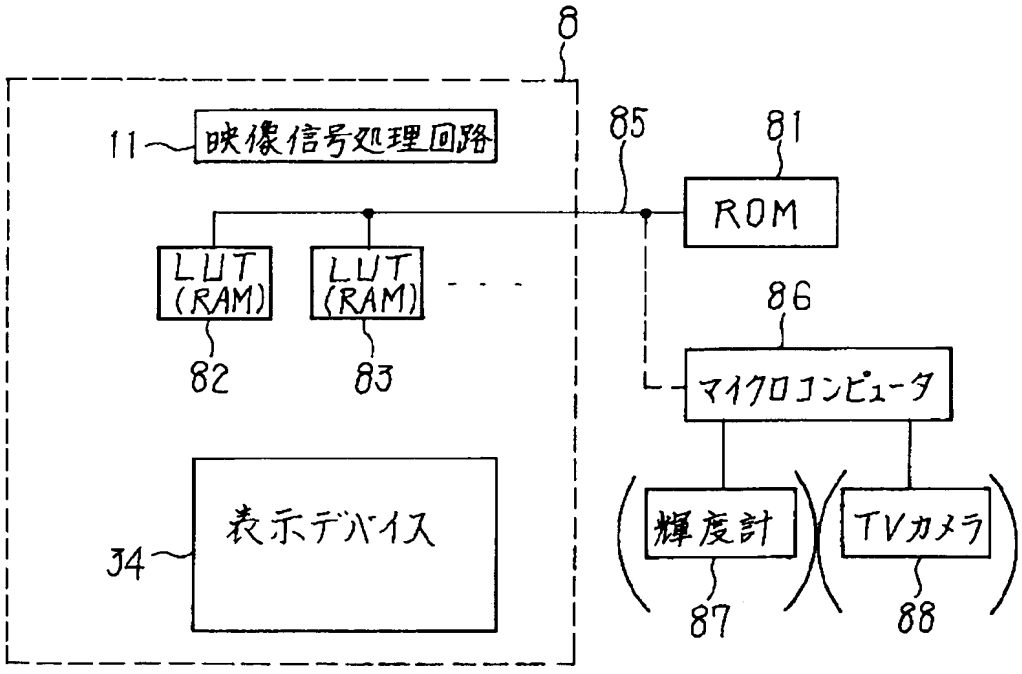
[Drawing 2]

図2



[Drawing 7]

図7



[Drawing 3]

図3

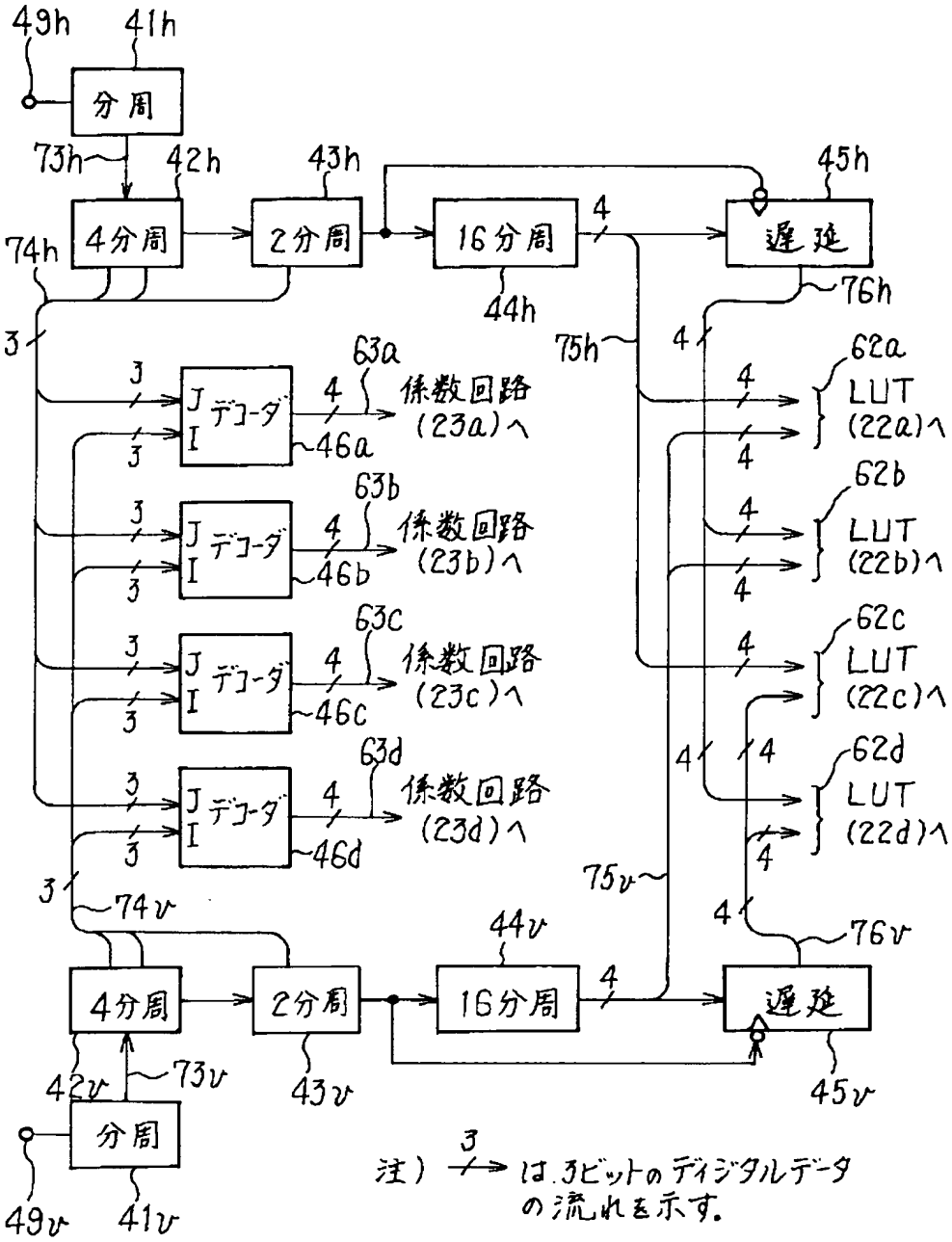
i＼j	0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	8 (000)	9 (001)
0 (000)	a_{00}	$\frac{3}{4}a_{00}$	$\frac{1}{2}a_{00}$	$\frac{1}{4}a_{00}$	0	$\frac{1}{4}a_{08}$	$\frac{1}{2}a_{08}$	$\frac{3}{4}a_{08}$	a_{08}	$\frac{3}{4}a_{08}$
1 (001)	$\frac{3}{4}a_{00}$	$\frac{9}{16}a_{00}$	$\frac{3}{8}a_{00}$	$\frac{3}{16}a_{00}$	0	$\frac{3}{16}a_{08}$	$\frac{3}{8}a_{08}$	$\frac{9}{16}a_{08}$	$\frac{3}{4}a_{08}$	$\frac{9}{16}a_{08}$
2 (010)	$\frac{1}{2}a_{00}$	$\frac{3}{8}a_{00}$	$\frac{1}{4}a_{00}$	$\frac{1}{8}a_{00}$	0	$\frac{1}{8}a_{08}$	$\frac{1}{4}a_{08}$	$\frac{3}{8}a_{08}$	$\frac{1}{2}a_{08}$	$\frac{3}{8}a_{08}$
3 (011)	$\frac{1}{4}a_{00}$	$\frac{3}{16}a_{00}$	$\frac{1}{8}a_{00}$	$\frac{1}{16}a_{00}$	0	$\frac{1}{16}a_{08}$	$\frac{1}{8}a_{08}$	$\frac{3}{16}a_{08}$	$\frac{1}{4}a_{08}$	$\frac{3}{16}a_{08}$
4 (100)	0	0	0	0	0	0	0	0	0	0
5 (101)	$\frac{1}{4}a_{80}$	$\frac{3}{16}a_{80}$	$\frac{1}{8}a_{80}$	$\frac{1}{16}a_{80}$	0	$\frac{1}{16}a_{88}$	$\frac{1}{8}a_{88}$	$\frac{3}{16}a_{88}$	$\frac{1}{4}a_{88}$	$\frac{3}{16}a_{88}$
6 (110)	$\frac{1}{2}a_{80}$	$\frac{3}{8}a_{80}$	$\frac{1}{4}a_{80}$	$\frac{1}{8}a_{80}$	0	$\frac{1}{8}a_{88}$	$\frac{1}{4}a_{88}$	$\frac{3}{8}a_{88}$	$\frac{1}{2}a_{88}$	$\frac{3}{8}a_{88}$
7 (111)	$\frac{3}{4}a_{80}$	$\frac{9}{16}a_{80}$	$\frac{3}{8}a_{80}$	$\frac{3}{16}a_{80}$	0	$\frac{3}{16}a_{88}$	$\frac{3}{8}a_{88}$	$\frac{9}{16}a_{88}$	$\frac{3}{4}a_{88}$	$\frac{9}{16}a_{88}$
8 (000)	a_{80}	$\frac{3}{4}a_{80}$	$\frac{1}{2}a_{80}$	$\frac{1}{4}a_{80}$	0	$\frac{1}{4}a_{88}$	$\frac{1}{2}a_{88}$	$\frac{3}{4}a_{88}$	a_{88}	$\frac{3}{4}a_{88}$
9 (001)	$\frac{3}{4}a_{80}$	$\frac{9}{16}a_{80}$	$\frac{3}{8}a_{80}$	$\frac{3}{16}a_{80}$	0	$\frac{3}{16}a_{88}$	$\frac{3}{8}a_{88}$	$\frac{9}{16}a_{88}$	$\frac{3}{4}a_{88}$	$\frac{9}{16}a_{88}$

( )内はjの下位3ビットを示す。

( )内はiの下位3ビットを示す。

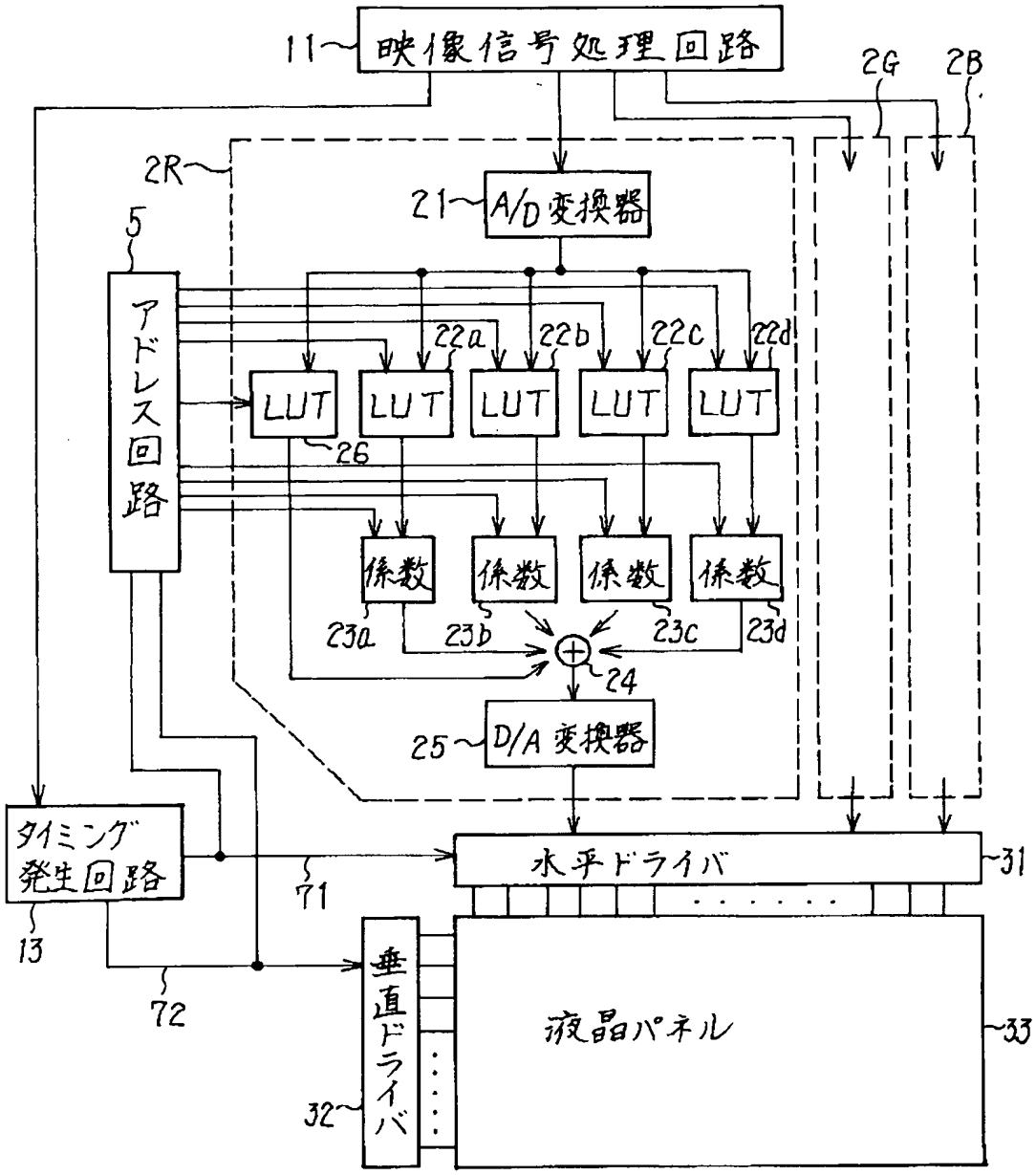
[Drawing 4]

図4


49h
41h
分周
73h
42h
43h
45h
4分周
2分周
16分周
遅延
74h
44h
76h
75h
63a
62a
Jデコーダ
I
係数回路
(23a)へ
46a
LUT
(22a)へ
63b
62b
係数回路
(23b)へ
46b
LUT
(22b)へ
63c
62c
係数回路
(23c)へ
46c
LUT
(22c)へ
63d
62d
係数回路
(23d)へ
46d
LUT
(22d)へ
74v
44v
76v
75v
4分周
2分周
16分周
遅延
42v
73v
43v
45v
分周
49v
41v
注) 3 → は3ビットのディジタルデータの流れを示す。

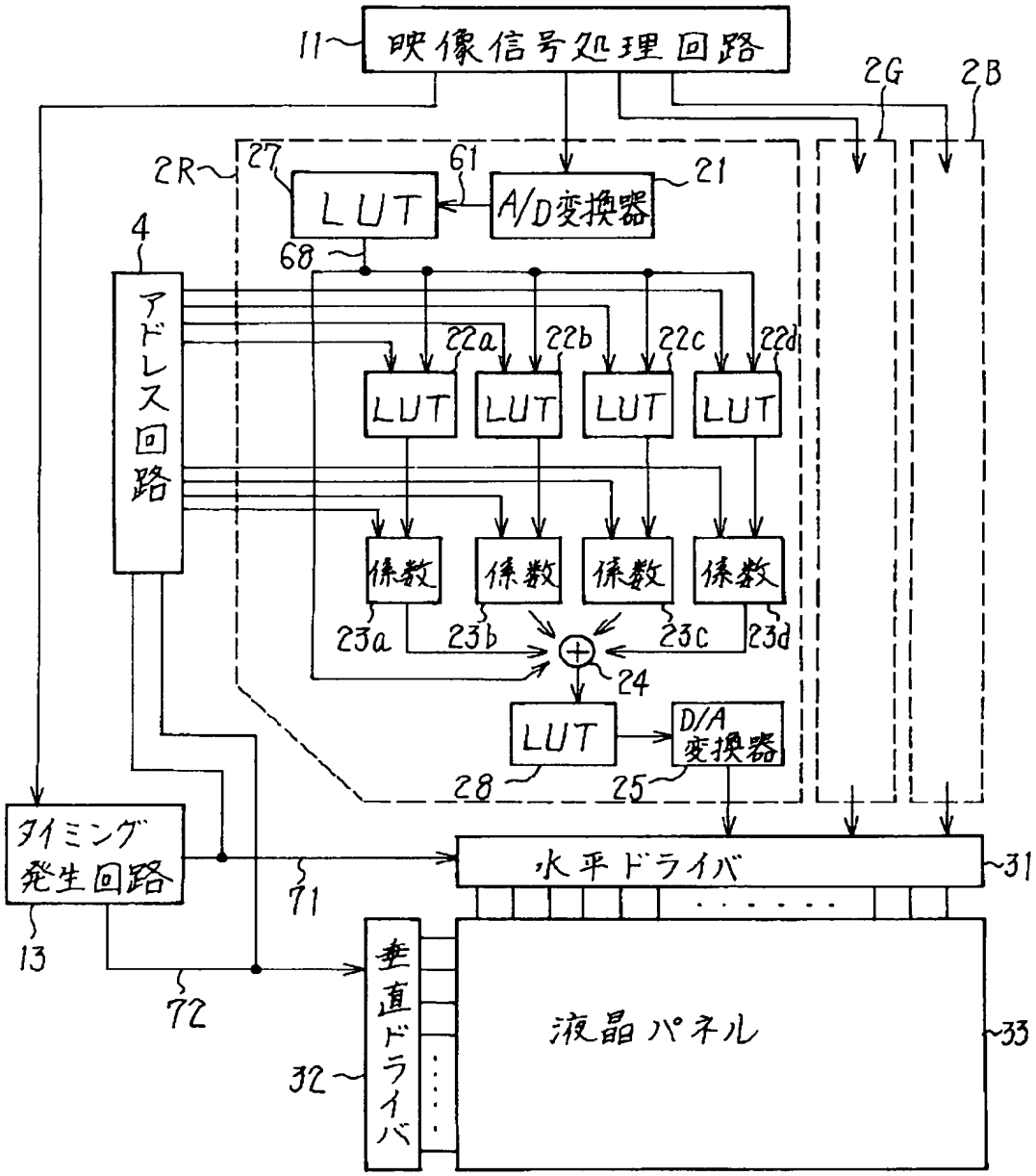
[Drawing 5]

図5


11
映像信号処理回路
2G
2B
2R
21
A/D変換器
5
アドレス回路
22a
22b
22c
22d
LUT
LUT
LUT
LUT
LUT
26
係数
係数
係数
係数
23a
23b
23c
23d
24
25
D/A変換器
タイミング発生回路
13
71
72
水平ドライバ
31
垂直ドライバ
32
液晶パネル
33

[Drawing 6]

図6



[Translation done.]